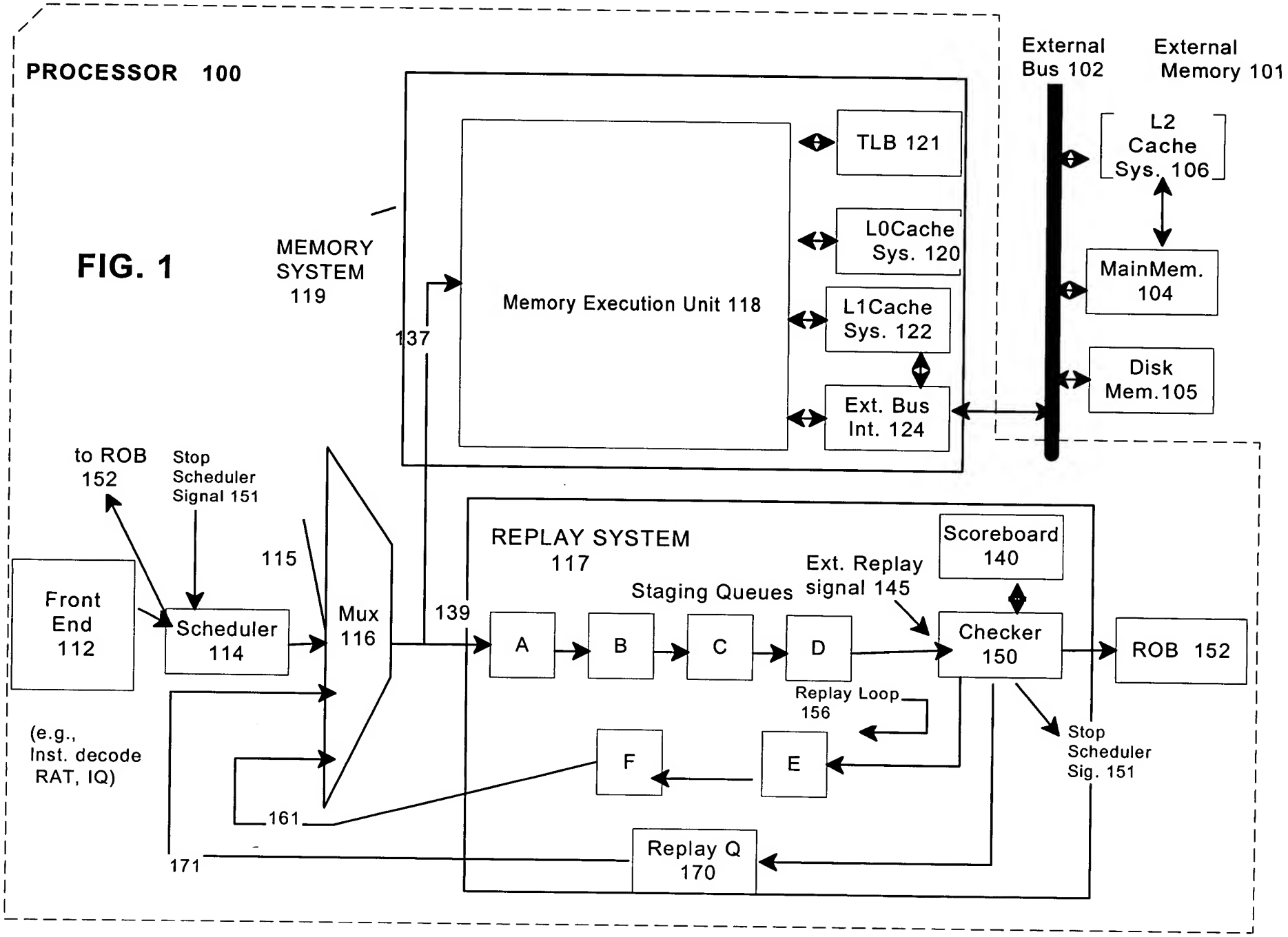
PROCESSOR 100
External Bus 102
External Memory 101
L2 Cache Sys. 106
MainMem. 104
Disk Mem.105
TLB 121
L0Cache Sys. 120
L1Cache Sys. 122
Ext. Bus Int. 124
Memory Execution Unit 118
MEMORY SYSTEM 119
137
FIG. 1
to ROB 152
Stop Scheduler Signal 151
115
Front End 112
Scheduler 114
Mux 116
139
REPLAY SYSTEM 117
Scoreboard 140
Ext. Replay signal 145
Staging Queues
A
B
C
D
Checker 150
ROB 152
Replay Loop 156
(e.g., Inst. decode RAT, IQ)
F
E
Stop Scheduler Sig. 151
161
171
Replay Q 170

72 SEQ. NO.	74 UOP	76 EXECUTED	78 Thread	80 PATH	82 RET	84 Exception/Fault Code (Vector)
N	OP	1	0	0	0	14 (e.g., Page Fault)
N+1	OP	0	0			
N+2	OP	0	1			
N+3	OP	0	1			

ROB 152

FIG. 2

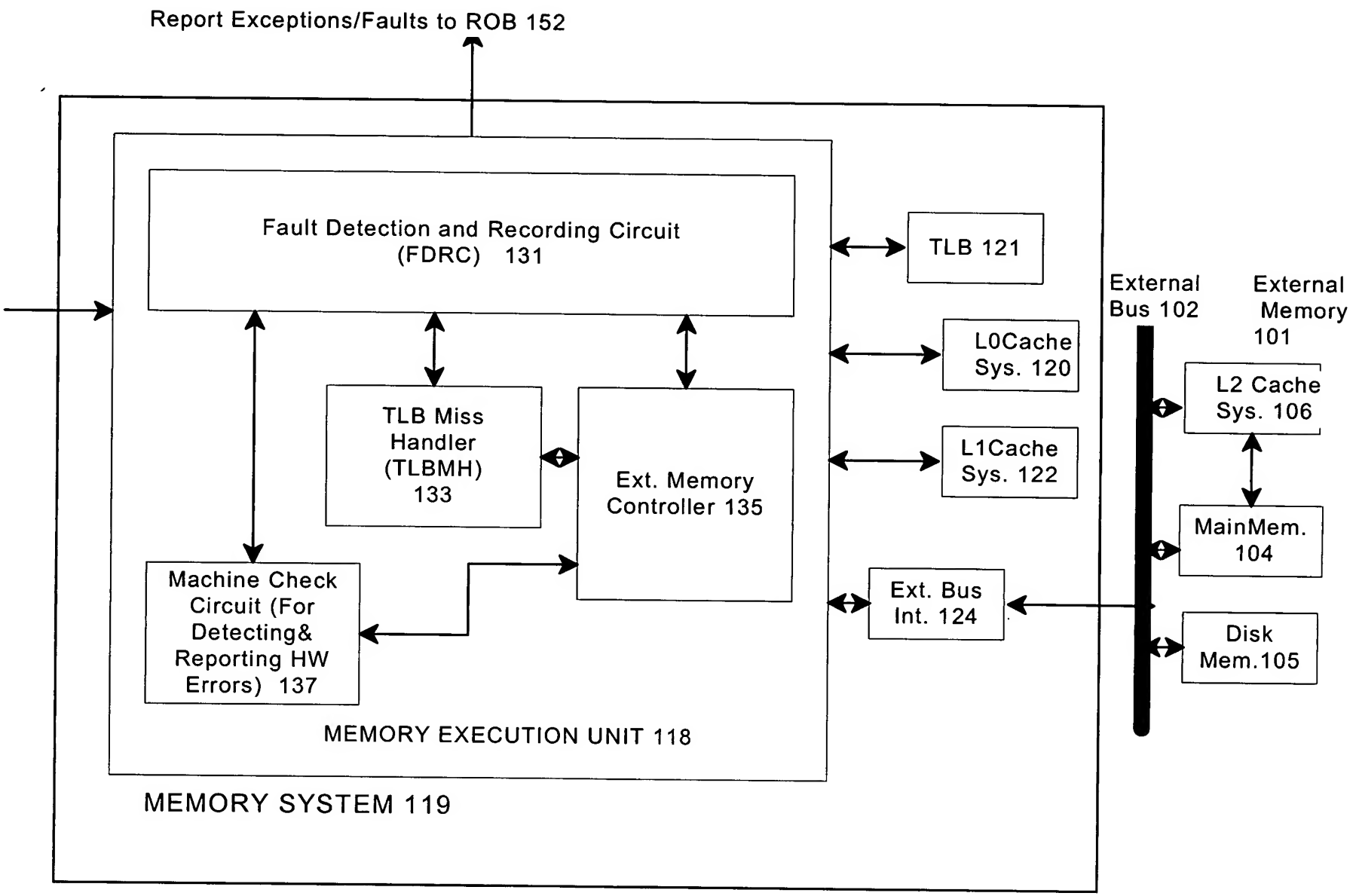
Report Exceptions/Faults to ROB 152
Fault Detection and Recording Circuit (FDRC) 131
TLB 121
L0Cache Sys. 120
L1Cache Sys. 122
TLB Miss Handler (TLBMH) 133
Ext. Memory Controller 135
Machine Check Circuit (For Detecting& Reporting HW Errors) 137
Ext. Bus Int. 124
MEMORY EXECUTION UNIT 118
MEMORY SYSTEM 119
External Bus 102
External Memory 101
L2 Cache Sys. 106
MainMem. 104
Disk Mem.105

FIG. 3

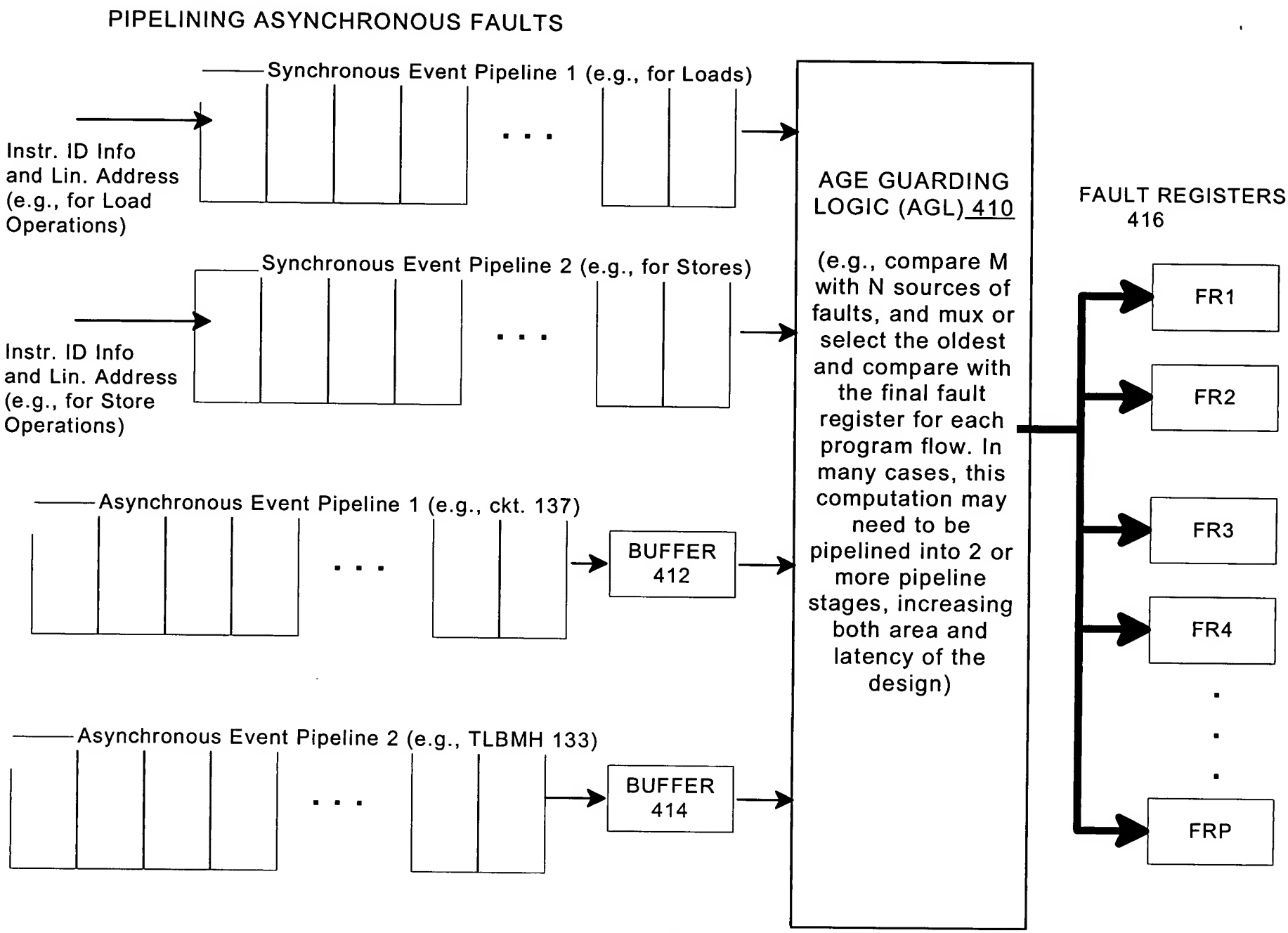
PIPELINING ASYNCHRONOUS FAULTS
Synchronous Event Pipeline 1 (e.g., for Loads)
Instr. ID Info and Lin. Address (e.g., for Load Operations)
Synchronous Event Pipeline 2 (e.g., for Stores)
Instr. ID Info and Lin. Address (e.g., for Store Operations)
Asynchronous Event Pipeline 1 (e.g., ckt. 137)
BUFFER 412
Asynchronous Event Pipeline 2 (e.g., TLBMH 133)
BUFFER 414
AGE GUARDING LOGIC (AGL) 410
(e.g., compare M with N sources of faults, and mux or select the oldest and compare with the final fault register for each program flow. In many cases, this computation may need to be pipelined into 2 or more pipeline stages, increasing both area and latency of the design)
FAULT REGISTERS 416
FR1
FR2
FR3
FR4
FRP

FIG. 4

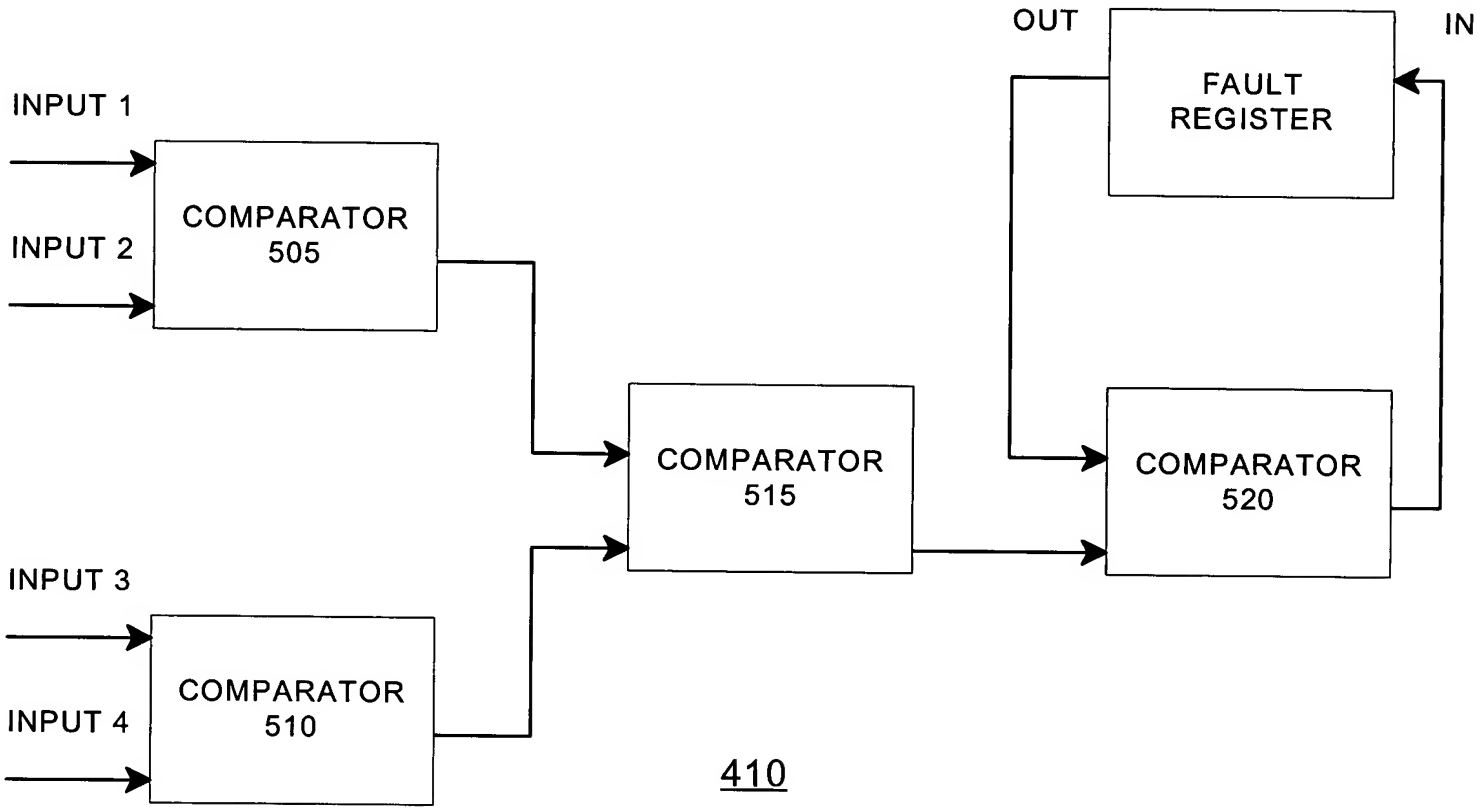
OUT
IN
FAULT REGISTER
INPUT 1
INPUT 2
COMPARATOR 505
COMPARATOR 515
COMPARATOR 520
INPUT 3
INPUT 4
COMPARATOR 510
410

FIG. 5

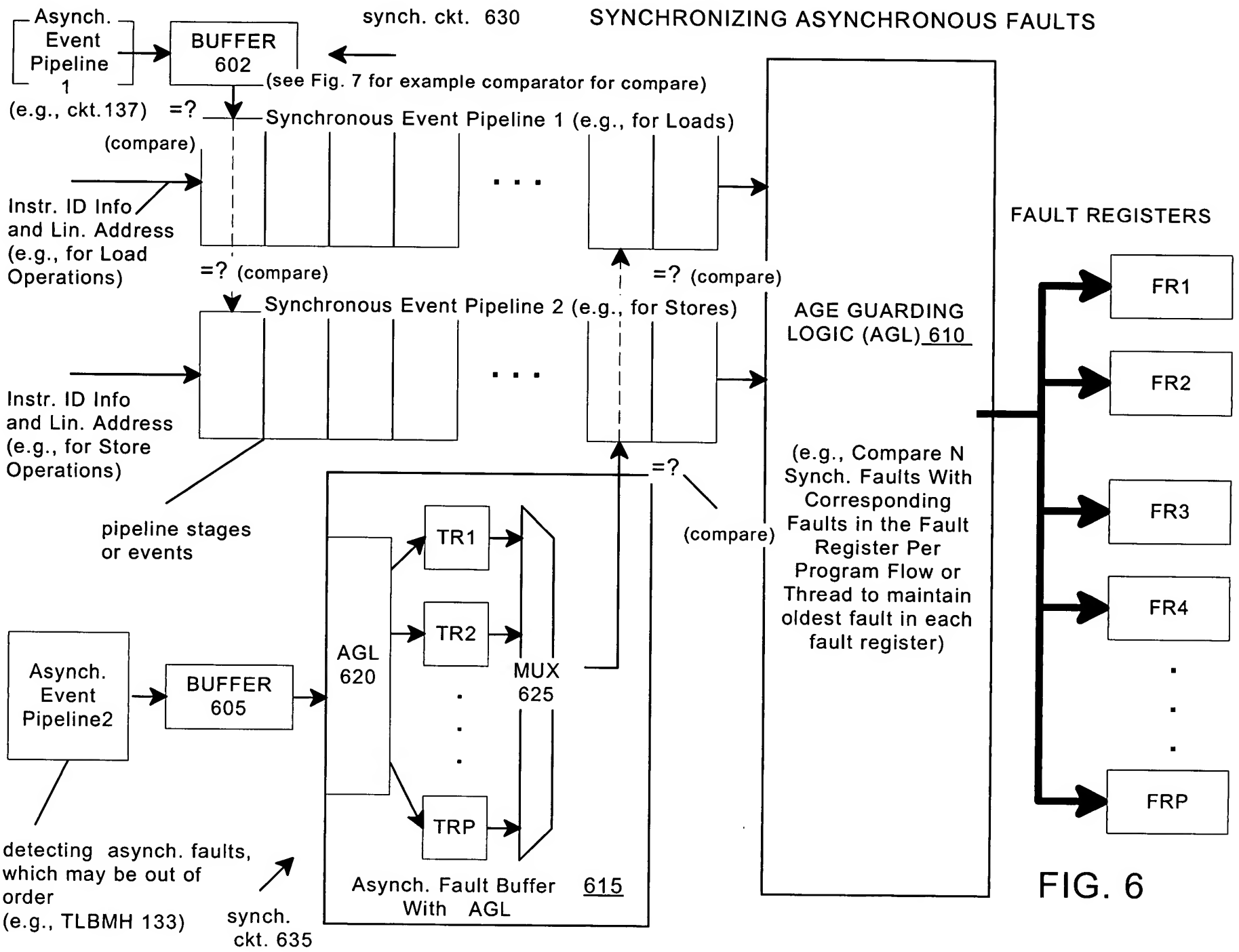
Asynch. Event Pipeline 1
(e.g., ckt.137)
BUFFER 602
synch. ckt. 630
SYNCHRONIZING ASYNCHRONOUS FAULTS
(see Fig. 7 for example comparator for compare)
=?
Synchronous Event Pipeline 1 (e.g., for Loads)
(compare)
Instr. ID Info and Lin. Address (e.g., for Load Operations)
=? (compare)
=? (compare)
Synchronous Event Pipeline 2 (e.g., for Stores)
AGE GUARDING LOGIC (AGL) 610
FAULT REGISTERS
FR1
FR2
FR3
FR4
FRP
Instr. ID Info and Lin. Address (e.g., for Store Operations)
pipeline stages or events
=?
(compare)
(e.g., Compare N Synch. Faults With Corresponding Faults in the Fault Register Per Program Flow or Thread to maintain oldest fault in each fault register)
TR1
TR2
TRP
AGL 620
MUX 625
Asynch. Event Pipeline2
BUFFER 605
detecting asynch. faults, which may be out of order
(e.g., TLBMH 133)
synch. ckt. 635
Asynch. Fault Buffer With AGL 615

FIG. 6

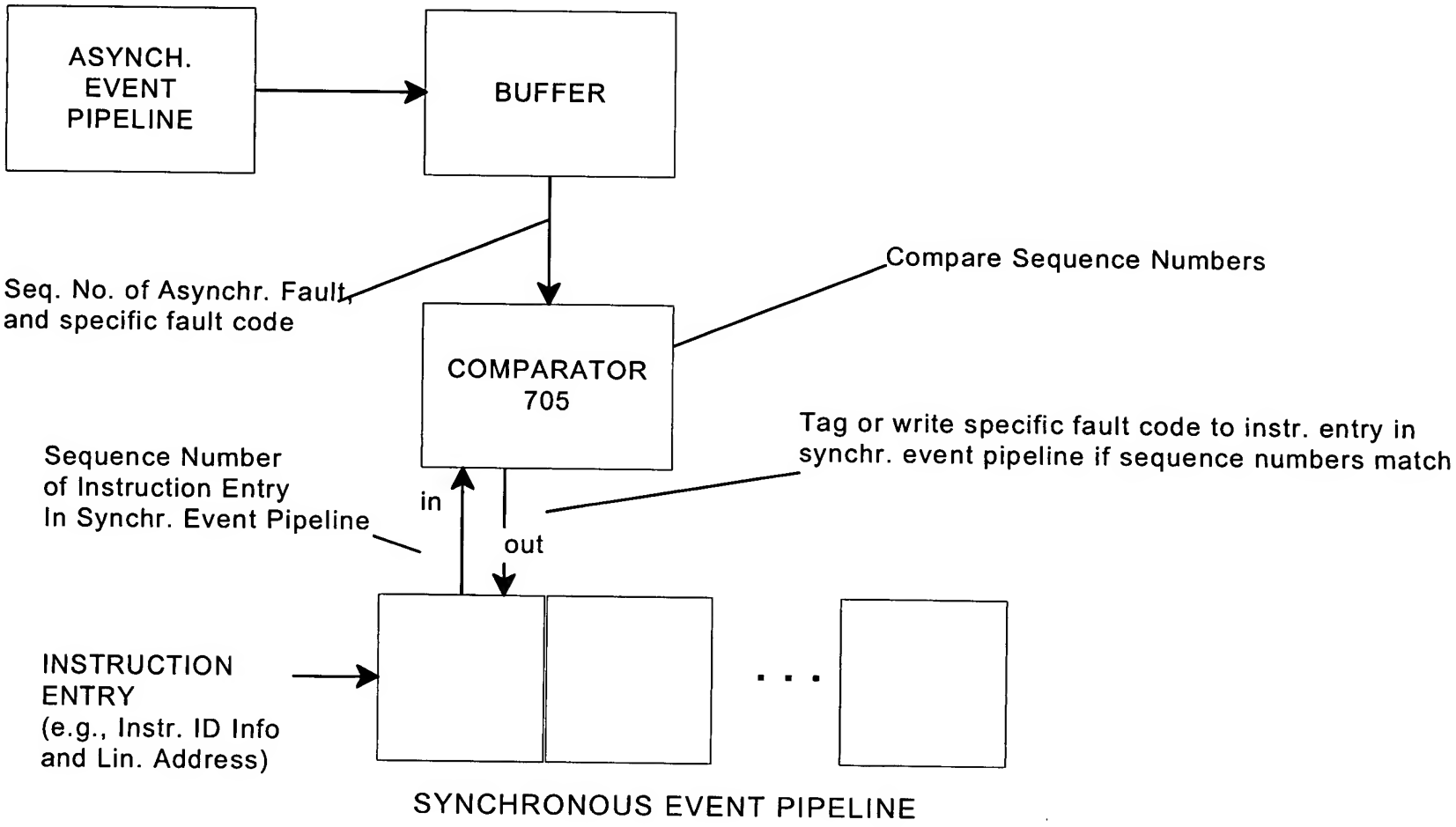
ASYNCH. EVENT PIPELINE
BUFFER
Seq. No. of Asynchr. Fault and specific fault code
Compare Sequence Numbers
COMPARATOR 705
Tag or write specific fault code to instr. entry in synchr. event pipeline if sequence numbers match
Sequence Number of Instruction Entry In Synchr. Event Pipeline
in
out
INSTRUCTION ENTRY (e.g., Instr. ID Info and Lin. Address)
SYNCHRONOUS EVENT PIPELINE

FIG. 7

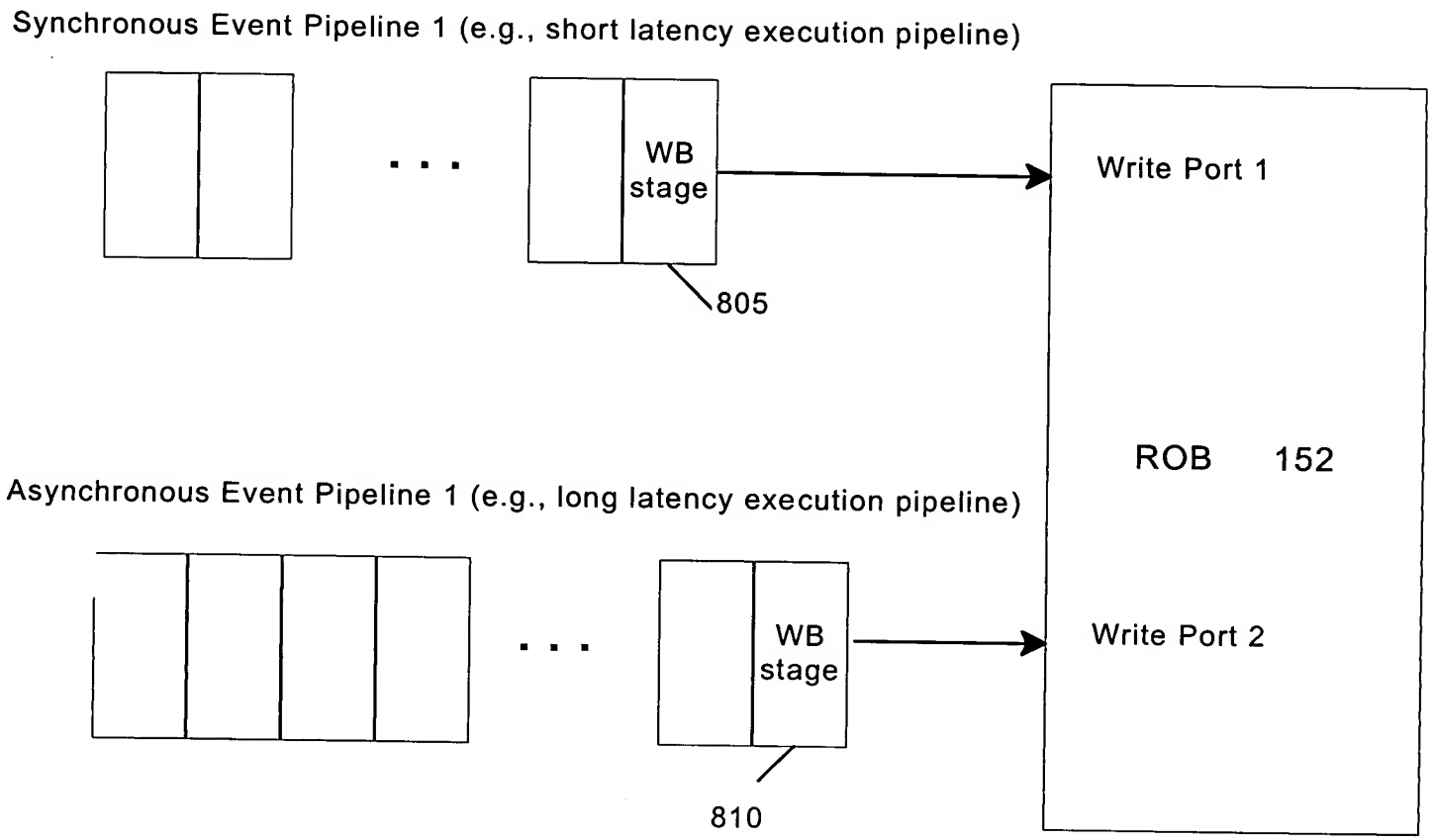
Synchronous Event Pipeline 1 (e.g., short latency execution pipeline)
WB stage
805
Write Port 1
ROB 152
Asynchronous Event Pipeline 1 (e.g., long latency execution pipeline)
WB stage
810
Write Port 2

FIG. 8

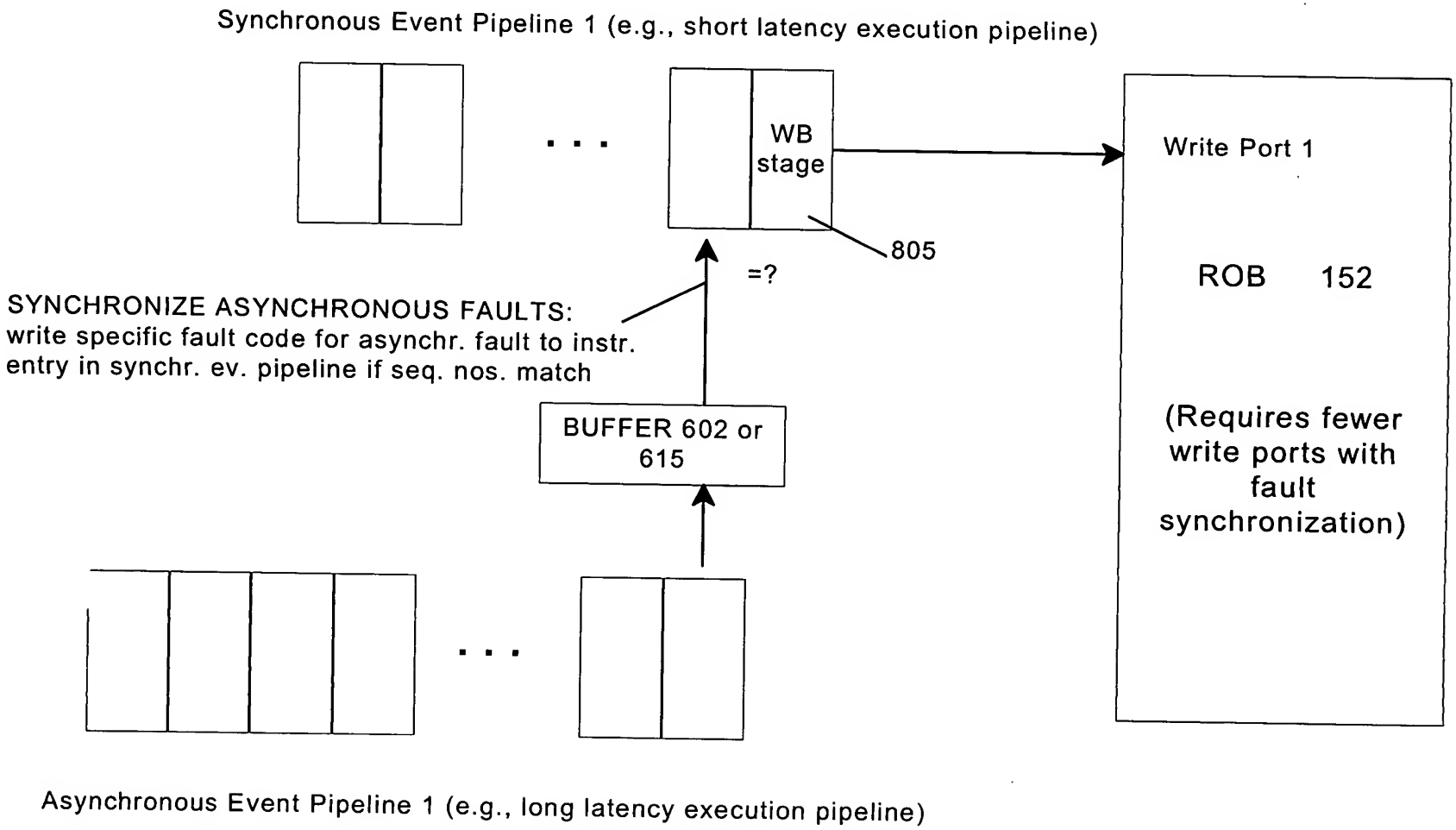
Synchronous Event Pipeline 1 (e.g., short latency execution pipeline)
WB stage
805
=?
Write Port 1
ROB 152
(Requires fewer write ports with fault synchronization)
SYNCHRONIZE ASYNCHRONOUS FAULTS:
write specific fault code for asynchr. fault to instr. entry in synchr. ev. pipeline if seq. nos. match
BUFFER 602 or 615
Asynchronous Event Pipeline 1 (e.g., long latency execution pipeline)

FIG. 9